What is claimed is:

1. A load activation and grace period timing system comprising:

a monitor for detecting when a lamp switch is activated and providing an output signal at a first level representative thereof;

a timer comprising a pulse generator and a counter, said counter receiving the output of said pulse generator, said timer receiving said output signal of said monitor to activate said pulse generator but to disable said timer so long as said first output signal is applied, said counter being enabled when said lamp switch is deactivated and said monitor output signal level changes to a second level, said counter counts said pulse generator output for a predetermined preset but variable time; and

a power switch for applying electrical power to said load when said monitor output signal is at said first level and continuing until said counter reaches said predetermined count.

2. A system as defined in claim 1 wherein said pulse generator is an analog oscillator including means for varying the frequency thereof, said frequency changes determining the variable grace period.

3. A system as defined in claim 2 wherein the system further includes a direct current power supply and said power switch comprises a field effect transistor.

4. A system as defined in claim 3 which further includes means for coupling said timer to said power switch for deactivating said power switch when said counter reaches said predetermined time of counting.

5. A system as defined in claims 4 wherein said counter generates a signal having one logic level when said lamp switch is activated and a second logic level when said counter reaches said predetermined time of counting.

6. A system as defined in claim 5 wherein means for coupling includes a transistor which conducts in saturation when said signal is at said one logic level to cause said field effect transistor to conduct and which is biased to its non-conducting state when said signal is at its second logic level to cause said field effect transistor to cease conducting.

7. A system as defined in claim 2 wherein the system further includes an alternating current power supply and said power switch comprises a Triac.

8. A system as defined in claim 7 which further includes an optocoupler for coupling said timer to said power switch for deactivating said power switch when said counter reaches said predetermined time of counting.

9. A system as defined in claim 8 wherein said counter generates a signal having one logic level when said lamp switch is activated and a second logic level when said counter reaches said predetermined time of counting.

10. A system as defined in claim 5 wherein means for coupling includes a transistor which conducts when said signal is at said one logic level to cause said optocoupler to conduct and generate a firing sequence of said Triac and which is biased to its non-conducting state when said signal is at its second logic level to cause said optocoupler to cease conducting and prevent said Triac from firing.